

# Controlled Transition Bridge Converter: Operating Principle, Control and Application in HVDC Transmission Systems

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**Abstract:** this paper employs an amplitude modulation with sinusoidal plus third harmonic injection instead of trapezoidal modulation to operate a controlled transition bridge (CTB) converter as ac/dc and dc/ac converter terminals. With such an operation, the CTB converter may require small ac filters; thus attractive for high-voltage direct current (HVDC) transmission systems. To facilitate ac voltage control over a wide range and black-start capability, the injected 3<sup>rd</sup> harmonic allows the cell capacitor voltages of the CTB converter to be regulated independent of the modulation index and power factor. The insertion of 3<sup>rd</sup> harmonic into modulating signals achieves two objectives: extends the regions around voltage zeros so that the total voltage unbalanced can be distributed between the cell capacitors, thereby exploiting the bipolar capability of the full-bridge cells in each limb; and to ensure that each limb can be clamped to the positive and negative dc rails every half fundamental period independent of the modulation index to allow recharge of the cell capacitors from the active dc link. The suitability of the CTB converter for HVDC type applications is demonstrated using a two-terminal HVDC link that employs a 21-cell CTB converter, considering normal operation and ac faults.

**Keywords:** High-voltage direct current transmission systems; two-level voltage source converter; modular multilevel converter; hybrid multilevel converter; fault-ride through capability; and black-start capability

## I. INTRODUCTION

Multilevel converters have found many applications at generation, distribution and transmission systems. This increasing trend started with the introduction of half and full bridge modular multilevel converters (HB-MMC and FB-MMC), which are well suited for high-voltage high-power applications [1-5]. Afterward, several multilevel converters were developed to overcome some of the main weaknesses of the MMCs such as: large footprint due to excessive use of cell capacitors, complex power circuit with many possibilities for malfunctions and high conversion losses should dc fault reverse blocking functionality is required [2, 6-17]. Among reverse blocking converters, mixed cell modular multilevel converter (MC-MMC) retains the elegance and modularity of the FB-MMC and offers relatively low semiconductor losses, without the drawbacks of the hybrid converters such as an alternative arm converter (AAC) and the hybrid cascaded two-level converters presented in [4, 18-25]. The majority of the MMC type converters proposed, such as those employing flying capacitor cells, three-level cells and five-level cells do not offer new features beyond those offered by the HB-MMC and MC-MMC [7, 26]. Therefore, these converters are less likely to be adopted in practical systems due to increased topology and control complexity. However, hybrid multilevel converters such as AAC and controlled transition bridge converter (CTB) have advantages over the FB-MMC and MC-MMC such as small footprint, competitive level of semiconductor loss, and high power density [20, 27]. However, their large input dc link capacitors for characteristic harmonic filtering is a major drawback that may hamper their applications in HVDC transmission systems; particularly, in multi-terminal HVDC networks. Amongst the non-reverse dc fault blocking converters (with the exception of the

conventional two-level converter), the CTB converter combines the lowest semiconductor loss and smallest footprint, which are attractive in applications with confined space requirements such as offshore wind farms and oil platforms. Reference [28] presented an alternative version of the CTB converter, in which the split dc link capacitors of the CTB converter are replaced by two blocks of full-bridge chain-links aim to achieve the following objectives:

- a) Avoids the increase of dc fault level during dc short circuit fault; as blocking of these additional chain links will be sufficient to stop discharge of the full-bridge cell capacitors to the dc fault.
  - b) The capacitance of the actively controlled cell capacitors could be increased in order to act as proper buffer between converter ac and dc side to ensure harmonic free continuous dc link current, without the adverse effect stated in (a).
- Thus, opening the way for the CTB converter to be applied to multi-terminal HVDC networks, instead of being limited to point-to-point HVDC links.

Nevertheless, the use of fourth leg (two chain links connected across the dc link) in the alternative version of the CTB converter compromises the main attributes of the original version of the CTB converter such as reduced footprint and losses.

The authors in [29] presented a full-bridge version of the CTB converter, where the full-bridge chain link of each phase must be rated for the full dc link voltage instead of half as in original version of the CTB converter. Also, the use of common dc inductor per three-phase in the dc link necessitates incorporation of an active device to circulate the stored energy in the dc link inductor in a zero voltage when the conduction path between converter and dc side is interrupted. This makes the full-bridge CTB converter less attractive in HVDC applications.

Reference [30] proposed a thyristor based CTB converter for ultra-high-voltage direct current (UHVDC) transmission systems, where the full-bridge chain links are exploited to enable forced commutation of the thyristors in the principle conduction path to further reduce semiconductor losses of the CTB converter to the level comparable to that of the conventional line commutated converter (LCC). Despite the switching limitations of thyristors employed in the main power stage, the CTB converter proposed in [30] is able to control active and reactive powers independently, and operate with zero dc power, while exchanging leading or lagging reactive power as any other voltage source converter. But it requires a number of large ac tuned filters to be able to achieve the desired voltage quality for grid operation.

References [31, 32] presented a hybrid converter that uses three limbs of cascaded half-bridge cells, which are connected across the positive and negative dc rail, and with each limb of cascaded half-bridge cells belongs to one phase-leg. Each limb of cascaded half-bridge cells is being exploited to generate a rectified dc voltage at the dc input of the high-voltage full-bridge converter of each phase-leg, which is responsible for synthesis of ac voltage to be imposed on the isolation transformer at the converter output. The cascaded half-bridge cells of each limb must be rated to block the maximum dc voltage equal to half of the dc link voltage, and composite (series connected) switching devices of each high-voltage full-bridge cell of each phase leg must be rated to block the maximum dc voltage of one limb (half of the dc link voltage), and switch at fundamental frequency and turn on and off zero voltage switching (ZVS). Given that the number half-bridge cells per phase in the hybrid converter in [31, 32] is equal to one-quarter of that of the MMC and no concentrated dc link capacitors, its space requirement is expected to be lower than that of the MMC and CTB of similar rating. However, lack of modulation index control (inability to vary ac voltage) of the hybrid converter in [31, 32] represents a major concern from the system prospective; particularly, inability to perform black-start and provision of reactive power during operation in ac grid. The above concerns have been addressed in the improved version of the above hybrid converter, which is refer to as series bridge converter (SBC) proposed in [33]. But the SBC has higher semiconductor losses and space requirement (footprint) compared to original version in [31, 32], but its footprint is expected to remain lower than that of the MMC, assuming the number of cell capacitors is a good indicator for converter volume.

This paper describes multilevel operation of a CTB converter and its modulation and control strategies that can facilitate operation independent of modulation index and power factor to be suitable for flexible ac transmission system (FACTS) devices

and HVDC transmission system applications. Open simulation waveforms show that 51-cells CTB converter can operate successfully with low and high modulation indices and power factors, with its cell capacitor voltages are tightly regulated. Furthermore, its suitability for FACTS devices and HVDC applications is assessed using a point-to-point VSC-HVDC link that employs 21-cell CTB converters, considering normal operation and ac network faults. The main conclusions drawn from this study, including key findings and observations are presented.

The rest of this paper is organized as follows: Section II discusses the basic operating principle of the CTB converter and its modulation and capacitor voltage balancing methods, and sizing of the cell capacitance. Also, it presents open loop simulations to support the theoretical discussions presented earlier. The test systems which will be used to assess the suitability of the CTB converter for dc transmission system and its control associated systems are described in Section III. Section IV provides comprehensive assessment of the CTB converter when applied to HVDC transmission systems, considering normal operation and ac fault. Section V compares the CTB converter to the half-bridge MMC considering a number of aspects, including semiconductor losses. The main conclusions of this paper are summarized in section VI.

## II. CONTROLLED TRANSITION BRIDGE (CTB) MULTILEVEL CONVERTER

### A) Basic Operating Principles

Fig. 1(a) shows the three-phase CTB converter proposed in [27]. Its circuit structure is similar to that of the T-type inverter discussed in, except that the series connected switches of the T-inverter between each output pole ( $a_o$ ,  $b_o$  and  $c_o$ ) and the neutral-point ( $O$ ) are replaced by the full-bridge chain links. A CTB multi-level converter with ' $N$ ' full-bridge cells per limb can generate ' $2N+1$ ' voltage levels per phase, between ( $a_o$ ,  $b_o$  and  $c_o$ ) and  $O$ . When a CTB converter is operated as suggested in [27], the switching devices of its main two-level bridge operate at the fundamental frequency and zero voltage swicthing; thus, negligible switching loss is incurred in this stage. Typically, the full-bridge chain link in each limb needs to block only half the dc link voltage ( $V_{dc}$ ); hence, the voltage across each cell capacitor must be maintained at  $\frac{1}{2}V_{dc}/N$ . This means the number of semiconductor devices in conduction path in each limb is  $N$ , which is the same as the main two-level bridge. As an example, for a CTB converter with a 640kV dc link voltage, employs 4.5kV IGBT with 55% utilization (2.5kV per IGBT at two-level bridge and chain links), the number of IGBT in the conduction path in each instant is 256 approximately and number of full-bridges cell per limb is 128. This an indication for low on-state loss of the CTB converter. The chain links and two-level bridge of the CTB converter in Fig. 1(a) operate in a complementary manner, with the full-bridge chain links of each phase being exploited to facilitate controlled transitions of the output voltage ' $v_{ao}$ ' between the positive and negative dc rails ( $+\frac{1}{2}V_{dc}$  and  $-\frac{1}{2}V_{dc}$ ), through intermediate voltage levels. Instead of using multi-slope trapezoidal modulation as suggested in [27], this paper uses modified sinusoidal modulation, which is created by injection an appropriate amount of 3<sup>rd</sup> harmonic into modulating signal of each phase, and this concept is borrowed from [34]. To ensure CTB cell capacitor balancing as the modulation index varies from 0 to 1.154, the injected 3<sup>rd</sup> harmonic must guarantee that the resulting modulating signal per phase has a unity peak, independent of fundamental modulating index,  $m$ , where,  $m = V_m / \frac{1}{2}V_{dc}$ , and  $V_m$  is the amplitude of the fundamental phase voltages  $v_{ao}$ ,  $v_{bo}$  and  $v_{co}$ . In this manner, the full-bridge cell capacitors of each limb will be clamped to the positive and negative dc rails every half fundamental period; thus, allowing controlled rebalancing of the full-bridge cell capacitors from the dc link. Fig. 2 shows the modulating signals being considered here for three different modulation indices. Observe that the injected 3<sup>rd</sup> harmonic extends the regions around the voltage zeros to allow both voltage polarities of the chain link cell capacitors to be manipulated in order to eliminate the voltage deviations from the desired set-point, as implemented in the cascaded two-level converter in [34, 35]. Notice that from the expression for the modulating signal for phase 'a'  $m_a(t) = m \sin \omega t + (1-m) \sin 3\omega t$ , the amount of the 3<sup>rd</sup> harmonic being injected into modulating signals varies over full modulation index linear range from '1' at  $m=0$  to -0.154 at  $m=1.154$ . Based on the aforementioned discussions, operation of the CTB converter can be divided into two modes:

- a) **Controlled transition mode:** This mode represents the period when the full-bridge cell capacitors of each limb are exclusively exploited to synthesize the intermediate output voltage levels between  $\frac{1}{2}V_{dc}$  and  $-\frac{1}{2}V_{dc}$ , and source or sink one third of the total active power the CTB converter exchanges with the ac side. Because of non-zero net energy exchange between the cell capacitors and ac side in this period, the cell capacitor voltages of the CTB converter will experience under-voltage or over-voltage (drift from the set-point), depending on the power flow direction.
- b) **Cell capacitor rebalancing mode:** This mode represents the periods when the upper or lower director switches of each phase are turned-on in order to allow the drift of the full-bridge cell capacitor voltages from the desired set-point to be corrected by clamping each limb to the positive or negative dc rail (forcing parallel operation of the limbs with the upper or lower dc link capacitors). In this way, the full-bridge cell capacitors will exchange additional rebalancing currents with the dc link to restore their voltages to the desired set-point. In this mode, all the ac power will be sourced from the dc link.

Theoretical substantiation of the above discussions is attempted using a simplified average model of the CTB converter in Fig. 1(b), assuming that the equivalent cell capacitor current is:

$$i_c(t) = m_a i_a \quad (1)$$

where phase 'a' output current ( $i_a$ ) is:  $i_a(t) = I_m \sin(\omega t + \varphi)$ ; phase 'a' modulation function  $m_a$  is:  $m_a = m \sin(\omega t + \delta) + (1-m) \sin 3(\omega t + \delta)$  [29, 34];  $\delta$  is the load angle between  $v_{ao}(t)$  at the converter terminal and grid voltage  $v_a(t)$ ;  $\varphi$  is the phase angle between  $v_a(t)$  and  $i_a(t)$ ;  $I_m$  is the output phase current peak; and  $m$  is the modulation index.

$$i_c(t) = \frac{1}{2} I_m [m \cos(\delta - \varphi) - m \cos(2\omega t + \delta + \varphi) + (1-m) \cos(2\omega t + 3\delta - \varphi) - (1-m) \cos(4\omega t + 3\delta + \varphi)] \quad (2)$$

Although the 3<sup>rd</sup> harmonic is injected into each per phase modulation signal to allow the output phase voltage ( $v_{ao}$ ) at converter terminal to be clamped to the positive and negative dc rails every half fundamental cycle, the equivalent cell capacitor current expressed by equation (2) contains a dc component that may lead to cell capacitor voltage drift from its set-point. This entails that the cell capacitor discharge would be avoided only if the equivalent cell capacitor were to draw a recharge current of  $-\frac{1}{2} m I_m \cos(\delta - \varphi)$  from the dc link every half fundamental cycle when each output phase voltage ( $v_{ao}$ ) is briefly and alternately clamped to the positive and negative dc rails. In this way, the average cell capacitor current over one or multiple fundamental period will be forced to zero. The peak recharge current that flows in each CTB limb is proportional to the active power being exchanged between dc and ac sides, where  $\cos(\delta - \varphi)$  represents power factor at the converter terminal. This indicates that the cell capacitor voltage drift is power factor dependent, with maximum and minimum drift at unity and zero power factors respectively.

From  $C_e \frac{dv_c}{dt} = i_c$  and equation(2), the equivalent cell capacitor voltage is approximated by:

$$v_c(t) = \frac{I_m}{2\omega C_e} \left[ \frac{m}{\pi} \cos(\delta - \varphi) \sin^{-1} \left( \sin \frac{1}{2} \omega t \right) - \frac{1}{2} m \sin(2\omega t + \delta + \varphi) + \frac{1}{2} (1-m) \sin(2\omega t + 3\delta - \varphi) \right] + K \quad (3)$$

where  $K = \frac{1}{2} V_{dc} + \frac{I_m}{4\omega C_e} [m \sin(\delta + \varphi) - (1-m) \sin(3\delta - \varphi) + \frac{1}{2} (1-m) \sin(3\delta + \varphi)]$ .

From equation (3), the cell capacitor voltage with  $N$  cells per limb can be approximated by:

$$v_{cap}(t) = \frac{v_c(t)}{N} = \frac{I_m}{2\omega C_e} \left[ \frac{m}{\pi} \cos(\delta - \varphi) \sin^{-1} \left( \sin \frac{1}{2} \omega t \right) - \frac{1}{2} m \sin(2\omega t + \delta + \varphi) + \frac{1}{2} (1-m) \sin(2\omega t + 3\delta - \varphi) \right] + \frac{1}{2} \frac{V_{dc}}{N} + \frac{I_m}{4\omega C_e} [m \sin(\delta + \varphi) - (1-m) \sin(3\delta - \varphi) + \frac{1}{2} (1-m) \sin(3\delta + \varphi)] \quad (4)$$

where the equivalent cell capacitance  $C_e = C/N$ ; and  $C$  is the submodule capacitance. The term  $I_m/4\omega C [m\sin(\delta + \varphi) - (1-m)\sin(3\delta - \varphi) + \frac{1}{2}(1-m)\sin(3\delta + \varphi)]$  in equation (4) must be eliminated by controlled recharge of the cell capacitors from the dc link.

### B) Cell Capacitance Sizing

Since the cell capacitors in each limb of the CTB converter must be capable of supplying or absorbing one third of rated active power during controlled transition period (which is approximately at least quarter of fundamental of period in the worst-case), while keeping cell capacitor voltage drift from the  $\frac{1}{2}V_{dc}/N$  to minimum; where,  $N$  is the number of cells per limb and  $V_{dc}$  is the dc link voltage. Using this energy conservation principle, the following equation can be defined:

$$\frac{1}{2}C_e [V_{c1}^2 - V_{c0}^2] = \frac{1}{3}P_0 \times \frac{1}{4}T \quad (5)$$

where  $V_{c0}$  represents the nominal equivalent cell capacitor voltage,  $V_{c1}$  stands for the equivalent cell capacitor voltage at the end of the controlled transition mode excluding the ac voltage ripple,  $T$  is the fundamental period, and  $P_0$  is the rated active power. If the voltage across the equivalent cell capacitor is allowed to drift from  $V_{c0}$  by  $k\%$ , then  $V_{c1}$  can be expressed as  $V_{c1} = (1 \pm k)V_{c0}$ . Therefore, the equivalent cell capacitance needed to keep the under-voltage of the cell capacitor voltage to minimum when the cell capacitors are sourcing or sinking rated active or dc power could be expressed as:

$$C_e = \frac{\frac{1}{6}P_0 \times T}{k[2 - k]V_{c0}^2} \quad (6)$$

Based on (6), the full-bridge cell capacitance needed is:

$$C = N \times \frac{\frac{1}{6}P_0 \times T}{k[2 - k]V_{dc0}^2} \quad (7)$$

Equation (7) provides the maximum theoretical value for the cell capacitance of the CTB that ensures the capacitor voltage ripple is bounded within  $\pm k\%$ . Since the cell capacitor voltage ripples exert additional voltage stresses on the semiconductor switches of the FB cells, the practical cell capacitance must be selected such that the cell capacitor voltage ripples should not exceed  $\pm 10\%$  of the rated voltage as in the conventional MMC[36]..

### C) Open Loop Illustration of the Main Features and Limitations

To corroborate the above discussions, simulation waveforms for a CTB converter when it operates in an open loop at low modulation index ( $m=0.65$ ), feeding a passive load are presented in Fig. 3. Simulation parameters used in this illustration are shown in the caption of Fig. 3. Fig. 3 (a) to (e) show that the CTB converter operates correctly and produces sinusoidal output currents and line-to-line voltage, and its cell capacitor voltages are tightly maintained around the set-point. Although the 3<sup>rd</sup> harmonic is observed in the phase voltage, it disappears in the line-to-line voltages in Fig. 3 (b) by common-mode effect; thus, leadings to sinusoidal output currents (this true as long as no path is provided for the zero sequence). Fig. 3 (b) shows samples of the voltage waveforms across phase 'a' upper switching device ( $S_{a1}$ ) and its corresponding limb voltage,  $V_{FB}$ . These waveforms show that the switching devices of the two-level stage such as  $S_{a1}$  operate at fundamental frequency, while the switching devices of the full-bridge cells in chain links are expected to operate at 150 Hz~200 Hz as in a typical half and full bridge MMCs. The gradual voltage build-up across the composite switches of the two-level converter stage such as  $S_{a1}$  and  $S_{a2}$ , allows the IGBTs in each string to be turned on and off individually; thus, stringent series connection of the IGBTs in  $S_{a1}$  and  $S_{a2}$  are not required. Given the low switching frequency and switch number in conduction path in each instant, the CTB multilevel converter is expected to have lower semiconductor losses compared to HB-MMC.

The main drawbacks of CTB converter when it operates in a full multilevel mode as proposed in this paper are:

- (i) Its switches are exposed to frequent and high inrush currents at the instances when its limbs are being clamped to the positive and negative dc rails in order to force rebalancing of the chain link cell capacitors of each limb.

- (ii) Its input dc link current discontinuity is worse than that of the AAC, thus, large reservoir capacitors are required at the dc input of the two-level converter stage.
- (iii) Requires large cell capacitance in order to keep the drift of the cell capacitor voltages from the desired set-point to minimum, and this is extremely important as it reduces the magnitudes of the limb inrush currents. To further limit the magnitude of the inrush or rebalancing currents of each limb shown in Fig. 3(f), the limb inductor must be sized properly.

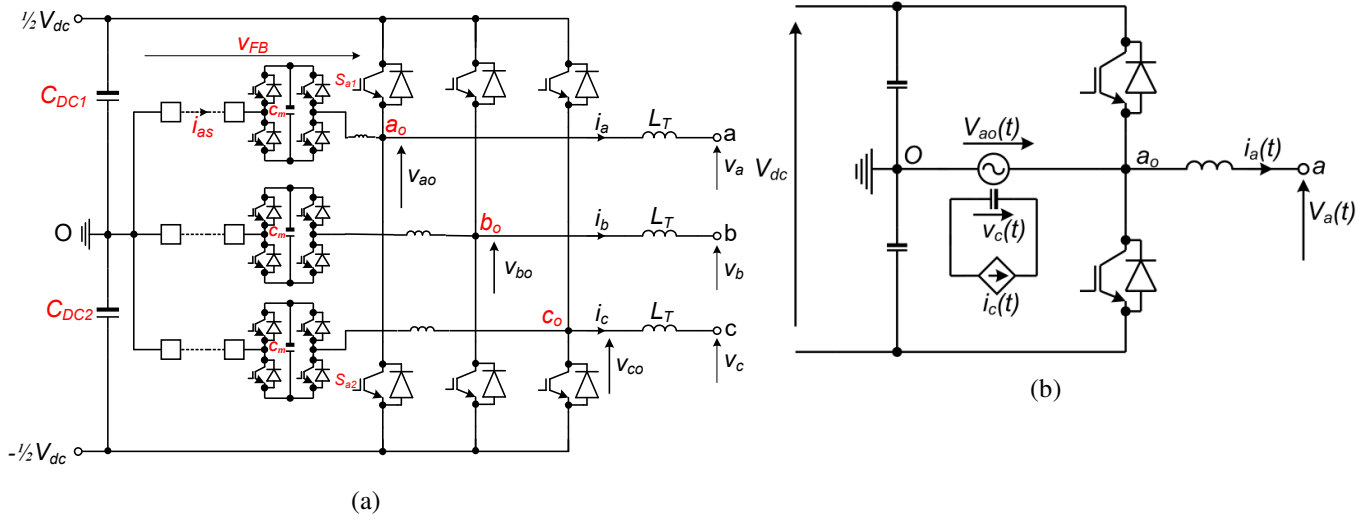


Fig. 1: (a) Three-phase controlled transition bridge multilevel converter, and (b) Per phase simplified model of the controlled transition bridge multilevel converter.

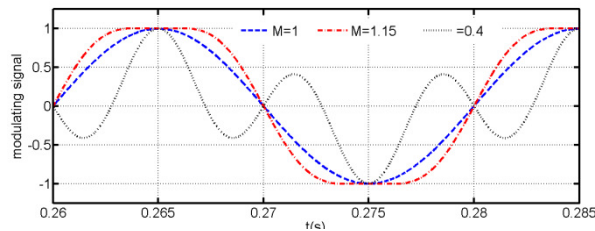
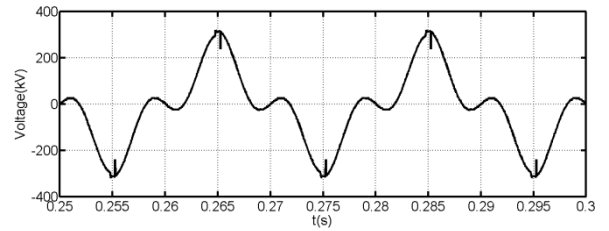
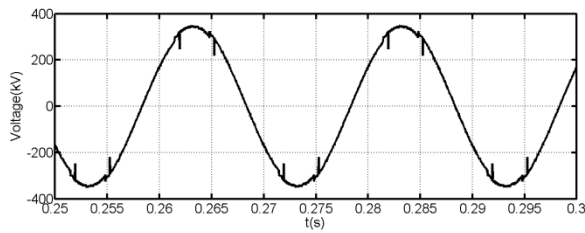


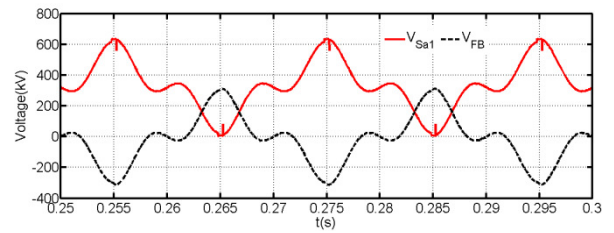
Fig. 2: Modulating signal of the CTB for different modulation indices ( $m=1, 1.15$  and  $0.4$ )



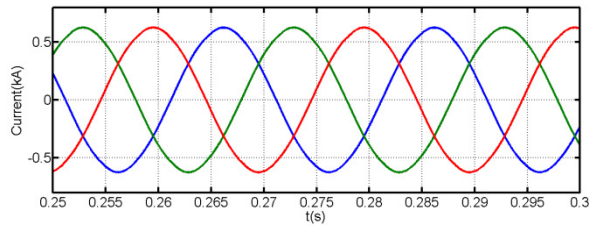
(a) Pre-filter phase voltage ( $v_{ao}$ )



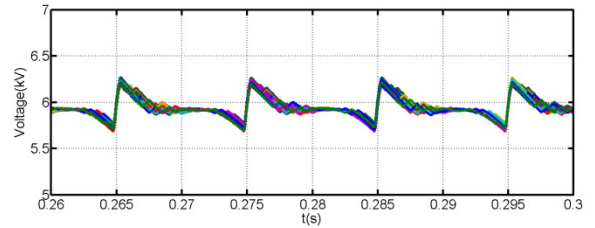
(b) Pre-filter line-to-line voltage measured at converter terminal



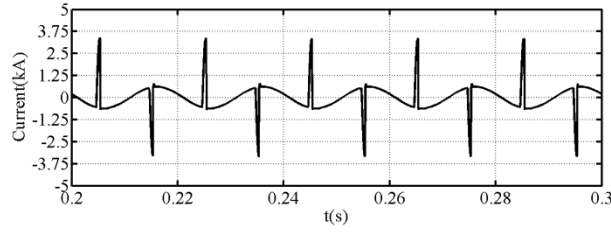
(c) Voltage waveforms across the upper switch ( $S_{a1}$ ) and chain link of phase 'a',  $V_{FB}$



(d) Three-phase output load currents



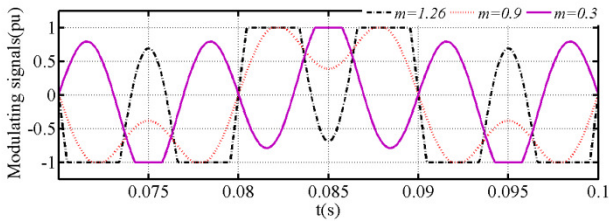
(e) Sample of the cell capacitor voltages of phase 'a'



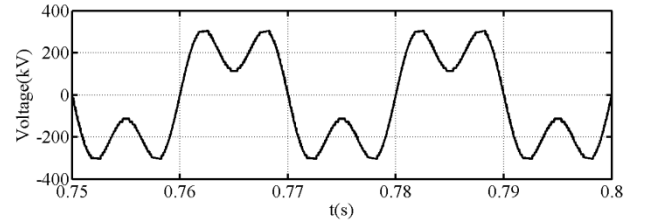
(f) Sample of the limb current (phase a)

Fig. 3: Waveforms that illustrate basic CTB operation with the proposed modified sinusoidal modulating signals ( $V_{dc}=\pm 320$  kV,  $N=51$ ,  $C_m=5$  mF,  $L_d=5$  mH,  $m=0.65$ , and load resistance and inductance are 300Ω and 314mH)

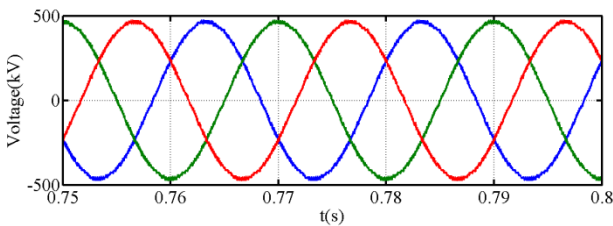
An alternative implementation of the proposed 3<sup>rd</sup> harmonic injection is  $v_a^*(t) = m \sin(\omega t + \delta) + m_3 \sin 3(\omega t + \delta)$ , where  $m_3 = (1 - m \sin \alpha) / \sin 3\alpha$  and  $\alpha = \cos^{-1} \frac{1}{4} \pi m$ . This approach reduces the inrush current in each limb (thus, losses during recharging of the cell capacitors) and temporary drift of the cell capacitor voltages as the modulation index decreases (because it extends the duration where each limb or output pole is clamped to positive and negative dc rails), see Fig. 4(a). Fig. 4(b) and Fig. 4(c) show the phase and line-to-line output voltages when CTB converter operates at 0.9 modulation index, feeding passive load with 0.31 power factor lagging. The plots for the output currents, cell capacitor voltages and limb currents in Fig. 4(d), (e) and (f) show that the CTB converter operates satisfactory, with all current and voltage stresses are tightly controlled. Despite the improved performance demonstrated in this section, the trapezoidal operation of CTB converter suggested in [27] is expected to outperform typical multilevel operation suggested in this paper from efficiency and cell capacitor energy storage requirement point of views (as the trapezoidal operating mode supplies most of the power directly from the dc link; thus, reduces the loading on the cell capacitors of the chain link). Nonetheless, these advantages of the trapezoidal operation are achieved at the expense of increasing ac filtering and limited modulation index control range[27].



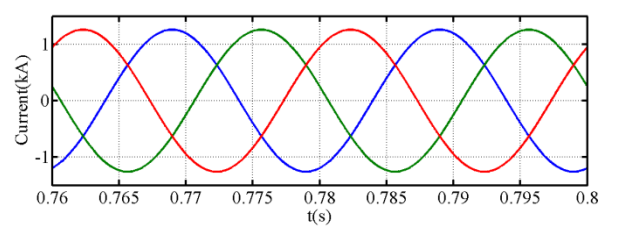
(a) Modulating signals for  $m=0.3$ , 0.9 and 1.26 with an alternative implementation of proposed 3<sup>rd</sup> harmonic injection



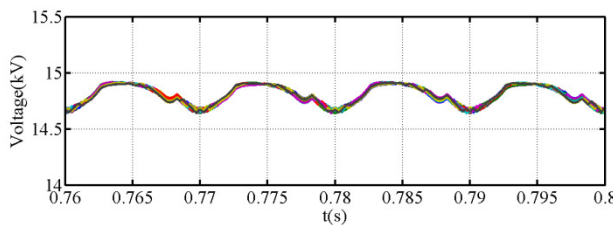
(b) Phase output voltage (vao)



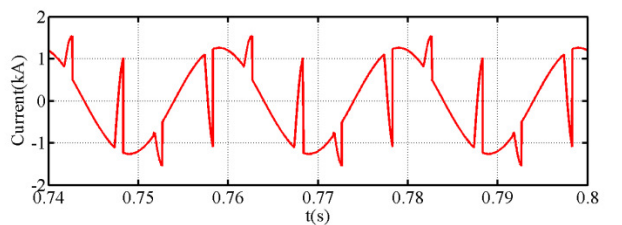
(c) Line-to line output voltage



(d) Three-phase output currents



(e) Cell capacitor voltages (phase 'a')



(f) Sample of the limb current in phase 'a'

Fig. 4: Waveforms with alternative implementation of the proposed 3<sup>rd</sup> harmonic injection (21-cell switch model of CTB converter,  $\pm 320$  kV dc link, 0.9 modulation index and 0.31 power factor lagging).



### III. TEST SYSTEM AND CONTROL SYSTEMS

Fig. 5 shows an illustrative two-terminal HVDC link this paper employs to assess the suitability of CTB converter for high-voltage applications, including its response to ac network faults. Its terminal converters VSC<sub>1</sub> and VSC<sub>2</sub> are modelled as CTB converter with 21 cells per limb in MATLAB-Simulink, and they regulate the active power and dc link voltage respectively, with unity power factors at B<sub>1</sub> and B<sub>2</sub>. Fig. 6 summarises the control systems used to control the CTB converters of the two-terminal HVDC link in Fig. 5. For detailed derivation of the control system in Fig. 6, see references [37]. Current limiting inductance in each limb is  $L_d=5\text{ mH}$ , where its internal resistance is lumped with switching device on-state resistance in  $R_d=0.25\ \Omega$ . Each full-bridge cell used in VSC<sub>1</sub> and VSC<sub>2</sub> has cell capacitance of  $C_m=3.4\text{ mF}$ . Both VSC<sub>1</sub> and VSC<sub>2</sub> employ staircase with nearest voltage level (amplitude) modulation and modified sinusoidal modulating signal described in section 0, and conventional capacitor voltage balancing that rely on sorting. To reduce the inrush current in each limb, a supplementary control loop that minimizes the mismatch between the dc link voltage and sum of the cell capacitor voltages of each limb is incorporated to Fig. 6. It maintains the cell capacitor voltages around the desired set-point and sets the reference charging currents for the inner controller that regulates the charging current of the FB cell capacitors and modifies the main modulating signals generated by the fundamental current controller in the  $d$ - $q$  frame, see Fig. 6. The differential equation that describes the ac voltage developed across each limb is:

$$\frac{d}{dt}(i_{abc} + \Delta i_{abc}) = -\frac{R_d}{L_d}(i_{abc} + \Delta i_{abc}) + \frac{(v_{abco} + \Delta v_{abco})}{L_d} \quad (8)$$

where  $i_{abc}$  and  $\Delta i_{abc}$  are the fundamental and cell capacitor charging currents in each limb and  $\Delta v_{abc}$  is the reference signal modification to ensure that the FB cell capacitors exchange zero active power with ac grid over one or several fundamental periods.

Equation (8) is separated into two parts; where the part of interest, which is related to the capacitor charging currents ( $\Delta i_{abc}$ ), is:

$$\frac{d}{dt}\Delta i_{abc} = -\frac{R_d}{L_d}\Delta i_{abc} + \frac{\Delta v_{abco}}{L_d} \quad (9)$$

The differential equation that describes cell capacitor dynamics is approximated as:

$$\frac{d}{dt}\bar{v}_{cap\_abc} = \frac{\Delta i_{abc}}{C_e} \quad (10)$$

where equivalent cell capacitance is  $C_e = C_m/N$  and the per phase average cell capacitor voltage is expressed as

$$\bar{v}_{cap\_abc} = \frac{1}{N} \sum_{j=1}^N v_{capj}^{abc}.$$

Equations (9) and (10) are used to design capacitor charging current and cell capacitor voltage regulators on a per phase basis:

$$\Delta i_{abc}^* = k_p (\Delta v_{cap\_abc}^* - \Delta v_{cap\_abc}) + k_i \int (\Delta v_{cap\_abc}^* - \Delta v_{cap\_abc}) dt \quad (11)$$

$$\Delta v_{abc}^* = \alpha_p (\Delta i_{abc}^* - \Delta i_{abc}) + \alpha_i \int (\Delta i_{abc}^* - \Delta i_{abc}) dt \quad (12)$$

After Laplace and matrix manipulations of the of the equations (9), (10), (11) and (12), the transfer functions for the cell capacitor voltage and limb current controllers are:

$$\frac{\bar{v}_{cap\_abc}(s)}{\bar{v}_{cap\_abc}^*(s)} = \frac{k_p/C_e s + k_i/C_e}{s^2 + k_p/C_e s + k_i/C_e} \quad (13)$$

$$\frac{\Delta i_{abc}(s)}{\Delta i_{abc}^*(s)} = \frac{\alpha_p/L_d s + \alpha_i/L_d}{s^2 + (\alpha_p + R_d)/L_d s + \alpha_i/L_d} \quad (14)$$



After comparison of the (13) and (14) with standard 2<sup>nd</sup> order transfer function, the gains for the outer cell capacitor voltage and inner limb current controllers are:  $k_p = 2\xi_1\omega_{n1}C_m/N$ ,  $k_i = \omega_{n1}^2C_m/N$ ,  $\alpha_p = 2\xi_2\omega_{n2}L_d - R_d$  and  $\alpha_i = \omega_{n2}^2L_d$ ; where  $\omega_{n1}$  and  $\omega_{n2}$ , and  $\xi_1$  and  $\xi_2$  are the outer and inner controllers' natural frequencies and damping factors respectively. These gains could be selected using time-domain specifications such as settling time, with the need to check the performance of these controllers in frequency domain in order to ensure they have adequate speeds for the task at hand and robustness to cope with external disturbances and uncertainties. Detailed procedures for derivation of the initial controller gains ( $k_p$ ,  $k_i$ ,  $\alpha_p$  and  $\alpha_i$ ) are explained in . These gains are further adjusted using time domain simulations in order to ensure satisfactory performance is achieved over all operating conditions, recognizing that the model based control design is unable to account for several fundamental factors and aspects such as dynamics associated with harmonic currents and voltages, and ac and dc network faults.

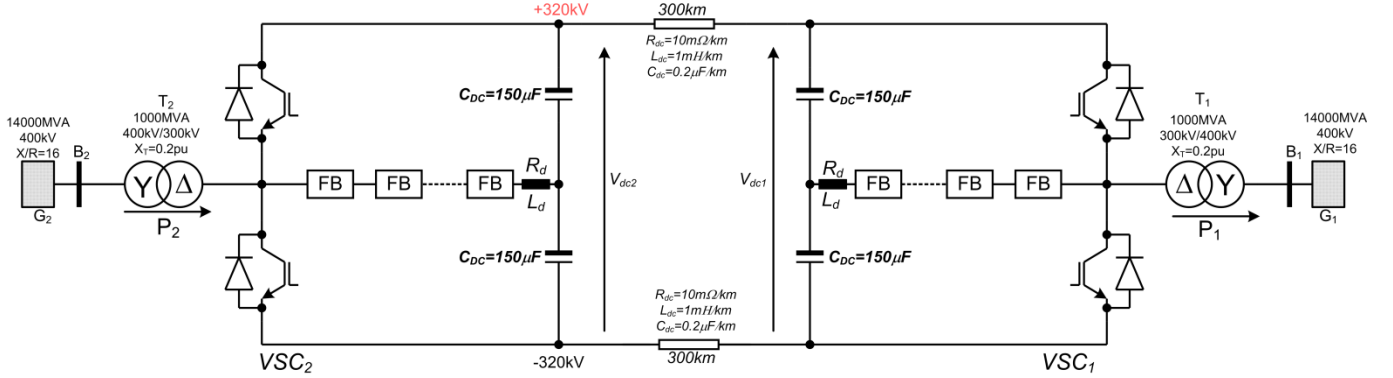


Fig. 5: Illustrative two-terminal HVDC link test system that uses cascaded transition bridge with 21 cells per limb,  $\pm 320\text{kV}$  dc link voltage, and VSC<sub>1</sub> and VSC<sub>2</sub> are designated as power and dc voltage regulators respectively.

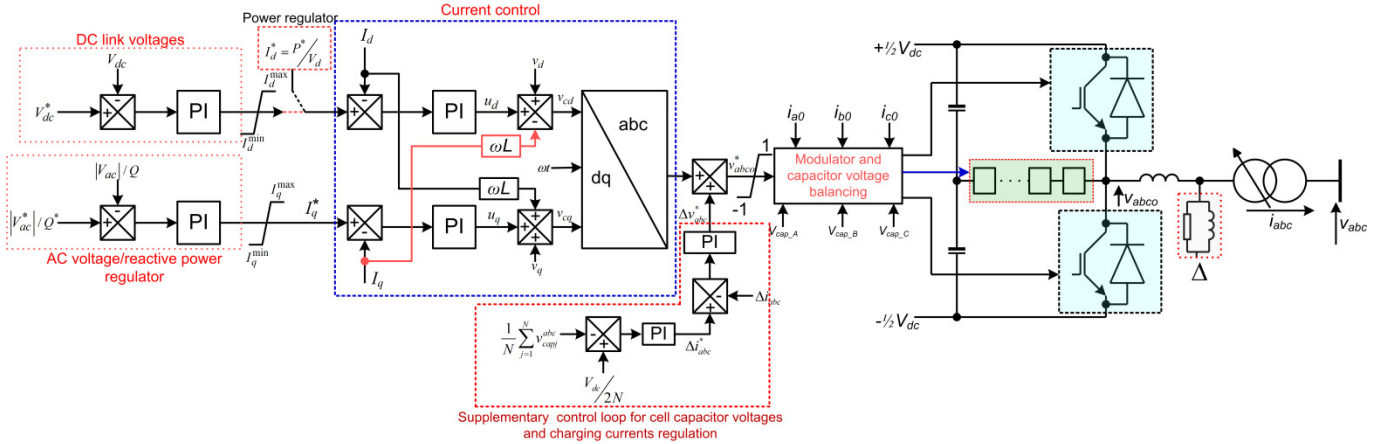


Fig. 6: Block diagram a generic control system used at VSC<sub>1</sub> and VSC<sub>2</sub>.

#### IV. PERFORMANCE EVALUATION

This section presents simulation cases that aim to illustrate the suitability of the CTB converter for HVDC transmission systems, considering normal operation and ac network faults.

##### (A) Normal operation

Initially, VSC<sub>1</sub> is commanded to exchange zero power between G<sub>1</sub> and G<sub>2</sub> (standby mode), and at  $t=0.5\text{ s}$ , VSC<sub>1</sub> ramps its output active power export from G<sub>1</sub> to G<sub>2</sub> from 0 to 800 MW and then the power flow direction is reversed at  $t=1.2\text{ s}$  (from 800 MW to -800 MW). VSC<sub>2</sub> is commanded to maintain the dc operating voltage of the system in Fig. 5 at  $\pm 320\text{ kV}$  (640 kV pole-to-pole). Simulation waveforms in Fig. 7 (a) and (b) show the active power VSC<sub>1</sub> and VSC<sub>2</sub> exchange with G<sub>1</sub> and G<sub>2</sub>, measured at B<sub>1</sub> and B<sub>2</sub>. Fig. 7 (c) and (d) are current waveforms VSC<sub>1</sub> and VSC<sub>2</sub> exchange with G<sub>1</sub> and G<sub>2</sub> at B<sub>1</sub> and B<sub>2</sub>. Fig. 7 (e) and (f) shows samples of the dc link voltages and current. Fig. 7 (g) and (h) show the cell capacitor voltages of the VSC<sub>1</sub> and VSC<sub>2</sub> are well regulated around  $\frac{1}{2}V_{dc}/N$  ( $320\text{ kV}/21 \approx 15.24\text{ kV}$ ). The CTB converters employed in the HVDC link in Fig. 5 exhibits good

dynamic performance, with active or dc power flow in both directions. The cell capacitance of  $C_m=3.4 \text{ mF}$  and equivalent dc link capacitance of  $75 \text{ } \mu\text{F}$ , which are equivalent to converter inertia:  $H = \left[ \frac{1}{2} C_{DC} V_{dc}^2 + 3 C_m V_{dc}^2 / 8N \right] / S_n \approx 40 \text{ ms}$ . This indicates that the dynamic performance of the CTB converter remains limited by the cell capacitor voltage dynamics as in all chain link topologies, including the achievable speeds for the power run-up and run-back, as the change of power set-point affects the energy level of the cell capacitors and of the dc link capacitors, see Fig. 7 (b), (g) and (h).

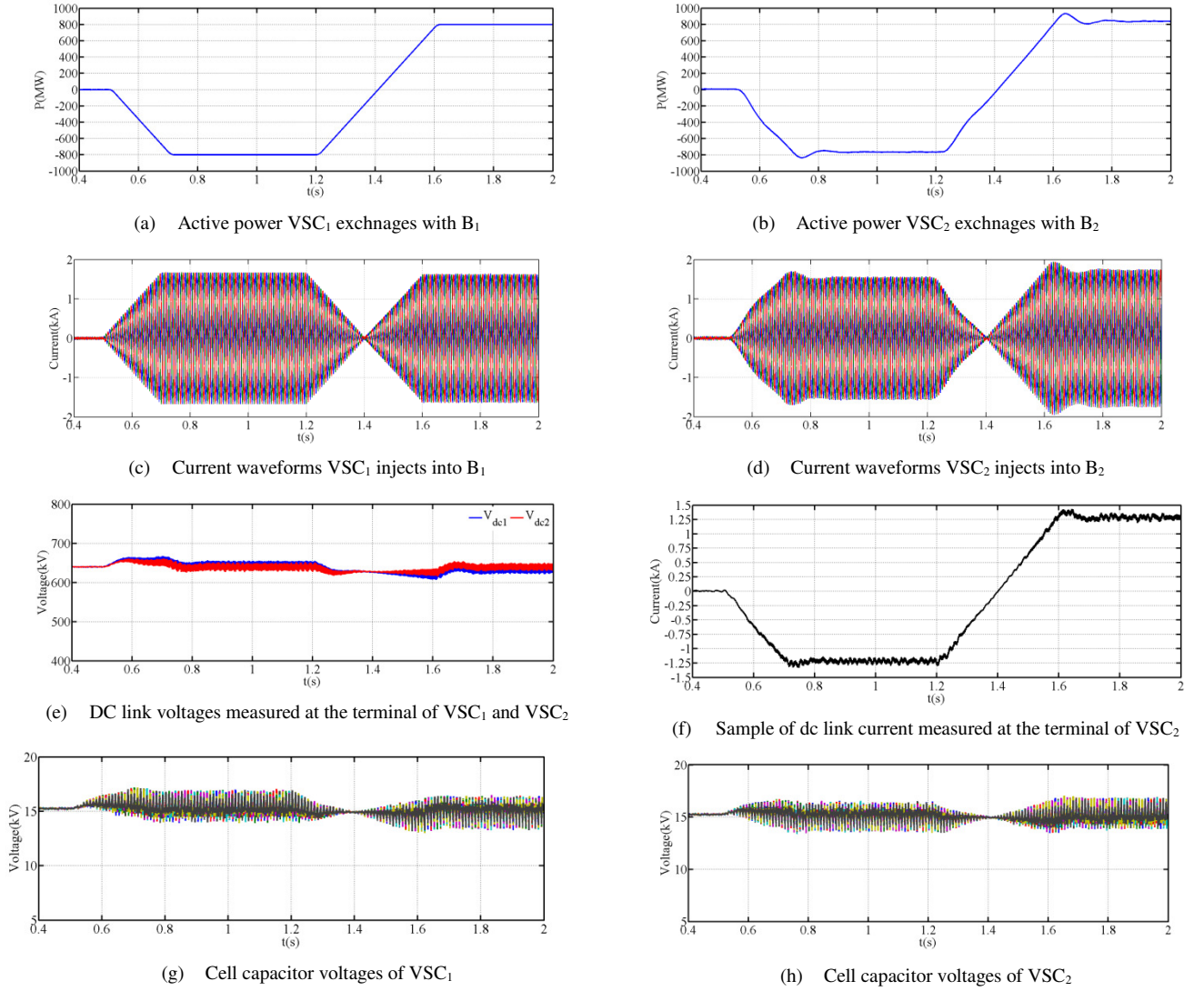
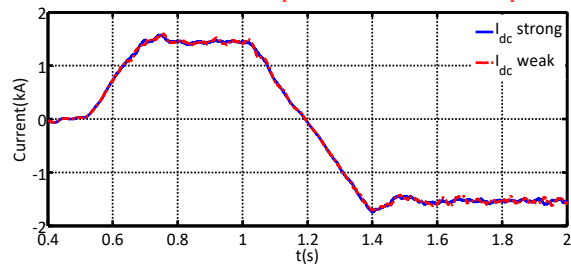


Fig. 7: Waveforms illustrating suitability of CTB converter in HVDC transmission system (normal operation).

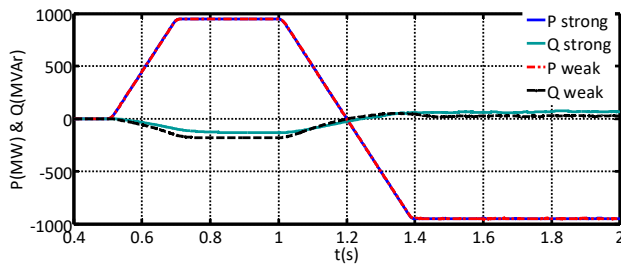
To demonstrate that the HVDC link based on the CTB converter can operate satisfactory in weak and strong ac grids, the illustrative test system in Fig. 5(a) is simulated assuming that: (1) strong ac grids at  $G_1$  and  $G_2$  with short circuit ratios  $SCR=10$ , and (2) weak ac grids at  $G_1$  and  $G_2$  with short circuit ratios  $SCR=4$ . Recall that the short circuit ratio (SCR) is defined as  $S_{3\phi}/P_{dc}$ , where  $S_{3\phi}$  and  $P_{dc}$  represent the ac grid three-phase short circuit fault level in MVA and converter rated dc power. In this illustration, VSC<sub>1</sub> is commanded to ramp-up the active power import (from  $G_2$  to  $G_1$ ) from 0 to 950 MW at  $t=0.5 \text{ s}$ . At  $t=1 \text{ s}$ , VSC<sub>1</sub> is commanded to reverse the power flow from 950 MW to -950 MW (exporting active power from  $G_1$  to  $G_2$ ). Both VSC<sub>1</sub> and VSC<sub>2</sub> are equipped with ac voltage controllers to maintain near constant ac voltages at  $B_1$  and  $B_2$ , which are critical for full exploitation of the converter power transfer capability,



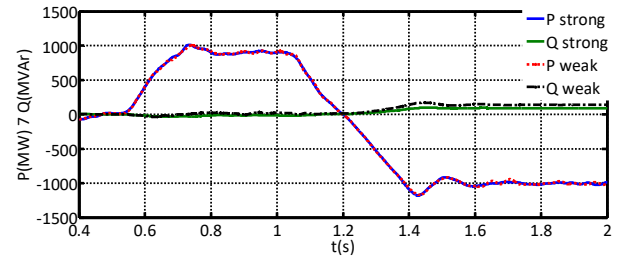
particularly, during operation in weak ac grids.

(a) DC link current

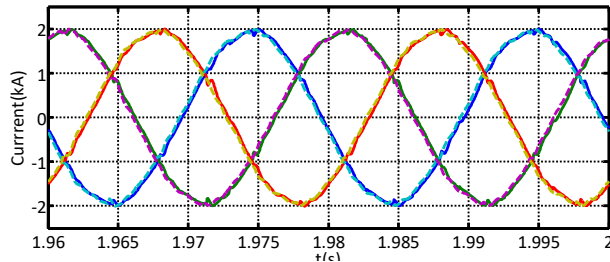
Fig. 8 (a), (b), (c), (d) and (d) display the active and reactive powers VSC<sub>1</sub> and VSC<sub>2</sub> exchange with the G<sub>1</sub> and G<sub>2</sub> at points of common coupling B<sub>1</sub> and B<sub>2</sub>, three-phase currents the converters VSC<sub>1</sub> and VSC<sub>2</sub> inject into B<sub>1</sub> and B<sub>2</sub>, and the dc link current, with the waveforms of the strong ac grids case are superimposed on that of the weak ac grids case. These simulation waveforms show that both CTB converters employed at VSC<sub>1</sub> and VSC<sub>2</sub> operate satisfactory with rated active power (considering both power flow directions) in strong ac grids with SCR=10 as well as in the weak ac grids with SCR=4. When the ac grids G<sub>1</sub> and G<sub>2</sub> are further weakened, for an example, SCR=3, the illustrative test system in Fig. 5(a) experiences sudden collapse when the dc or active power being transmitted exceeds 85% of the rated power. It is worth emphasizing that this problem is well known when the voltage source converters operate in weak ac system and extensively investigated [38, 39]. But this is beyond the scope of this paper.



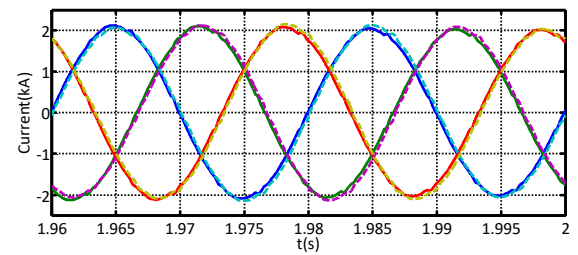
(b) Active and reactive powers VSC<sub>1</sub> exchanges with G<sub>1</sub> at B<sub>1</sub>



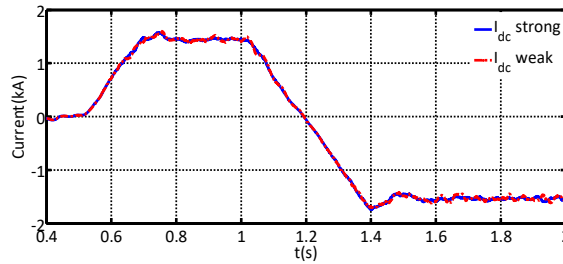
(c) Active and reactive powers VSC<sub>2</sub> exchanges with G<sub>2</sub> at B<sub>2</sub>



(d) Three-phase currents VSC<sub>1</sub> injects into B<sub>1</sub>



(e) Three-phase currents VSC<sub>2</sub> injects into B<sub>2</sub>



(f) DC link current

Fig. 8: Simulation waveforms that illustrate the performance of the CTB converter based HVDC link during operation in strong and weak ac grids, with the waveforms of the strong ac grid case are superimposed on their equivalent from the weak grid case

### (B) AC network fault

To assess CTB converter ac fault ride-through [capability](#), the test system in Fig. 5 is subjected to a temporary three-phase ac fault at B<sub>1</sub>, with 100ms fault duration. During the fault period, the converter output power is reduced to zero. Fig. 9 (a) and (b) show the voltage and current waveforms at B<sub>1</sub>, zoomed around the fault period. Observe that the CTB converter is able to ride-through the ac fault with its current control fully functional as with other established voltage source converters. In this illustration, an autonomous ac voltage support control loop is not incorporated; rather the reactive power demand is set to zero. Should an ac voltage controller be incorporated, some limited reactive power current will be observed in Fig. 9(b). With power flow from G<sub>1</sub> to G<sub>2</sub> (active power controller 'VSC<sub>1</sub>' to dc voltage controller 'VSC<sub>2</sub>'), a sudden active power reduction (fast power run-back) results in instantaneous reduction of ac power (ac current in Fig. 9b) but not in the dc power (dc link current in Fig. 9c). This creates temporary power imbalance between the ac and dc side as the cell capacitors of both terminals attempt to adjust their

energy levels to achieve zero dc power. The plots for the VSC<sub>2</sub> dc link voltage and cell capacitor voltages in Fig. 9(d), (e) and (f) show a dip in their dc voltages when the ac power is reduced; this is because the dc link and cell capacitors have to compensate for the power mismatch until power balanced between the ac and dc sides is restored. Such phenomenon existed in all chain link topologies [37]. Therefore, it must be accounted for when sizing the cell capacitor voltages to avoid excessive voltage stresses on the cell capacitors and switching devices when the power flow direction is reversed rapidly or reduced to zero.

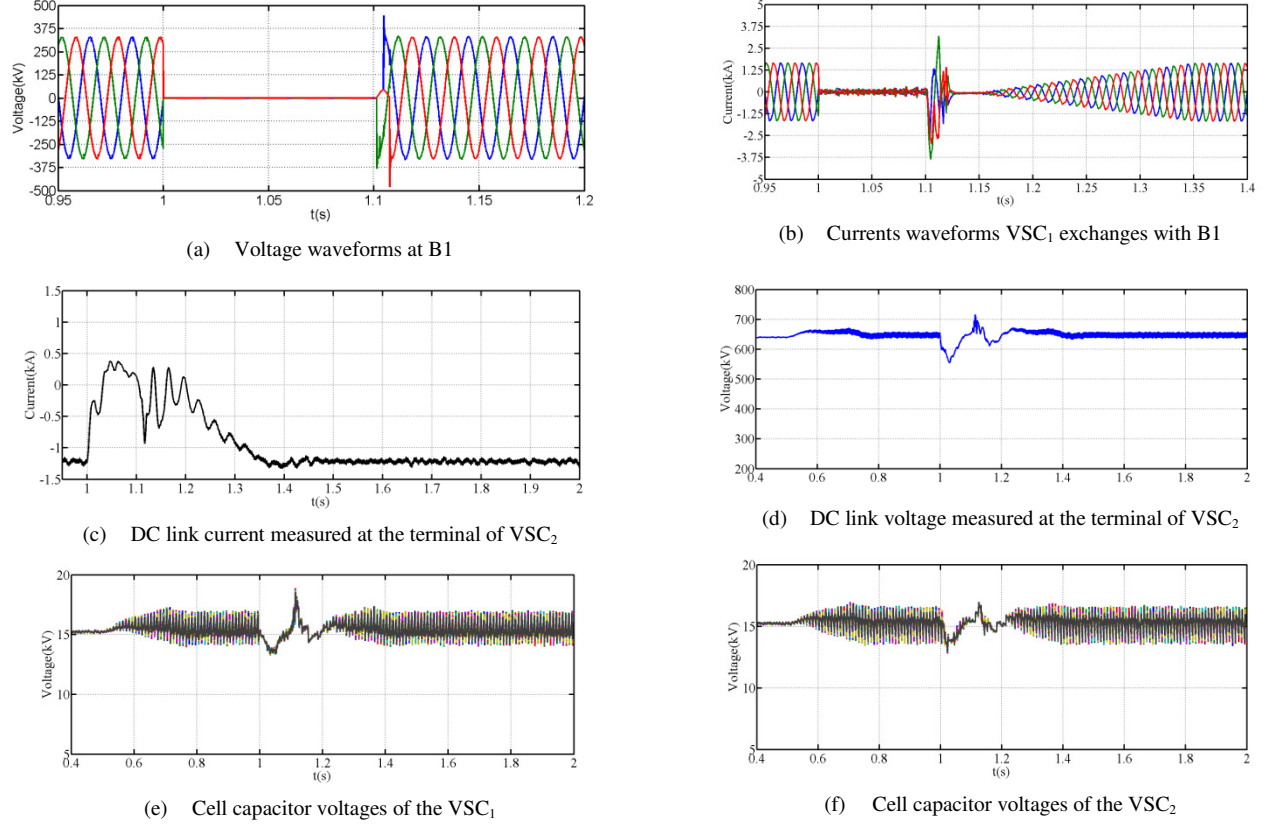


Fig. 9: Waveforms demonstrating the resiliency of the CTB converter based HVDC links to ac network fault.

### (C) Pole-to-pole dc short circuit fault

Fig. 10 presents simulation waveforms when the CTB converter based HVDC link in Fig. 5 is subjected to a permanent pole-to-pole dc short circuit fault at the middle of the dc line that connects the converter terminals VSC<sub>1</sub> and VSC<sub>2</sub> at  $t=0.9s$ . In pre-fault the condition, the active power controlling converter VSC<sub>1</sub> imports 800MW from G<sub>2</sub> to G<sub>1</sub>, and both converter terminals VSC<sub>1</sub> and VSC<sub>2</sub> are blocked after 50 $\mu s$  from the instant of the dc fault inception. The traces for the three-phase ac currents VSC<sub>1</sub> and VSC<sub>2</sub> inject into B<sub>1</sub> and B<sub>2</sub>, and dc link voltage and current at the dc terminals of the VSC<sub>1</sub> in Fig. 10 (a) and (b), (c) and (d) show that the CTB converters employed at VSC<sub>1</sub> and VSC<sub>2</sub> exhibit similar behaviours to that of the conventional two-level converter and half-bridge MMC. For an example, the loss of control when its dc link voltage falls below the critical voltage (the peak of the line-to-line ac voltage the interfacing transformers impose at ac terminals of the VSC<sub>1</sub> and VSC<sub>2</sub>); hence leading to significant ac current in-feeds from the ac grids G<sub>1</sub> and G<sub>2</sub>. The loss of controllability happens because the ac voltages being imposed at the ac terminals of the VSC<sub>1</sub> and VSC<sub>2</sub> (by the ac grids G<sub>1</sub> and G<sub>2</sub>) will force the freewheeling diodes of the main two-level converter stage to be forward biased even when the CTB converter is blocked (all switching devices are gated off). However converter blocking remains critically important for protection of the IGBT parts of the composite switching devices as in all non-reverse blocking converters such as the conventional two-level converter and half-bridge MMC. Simulation waveforms for the full-bridge cell capacitor voltages in Fig. 10 (e) and (f) show that the blocked full-bridge cells present sufficient counter-voltage which forces the current flow in each limb of the CTB converter to zero (this can be seen in the flatness of the cell capacitor voltages).

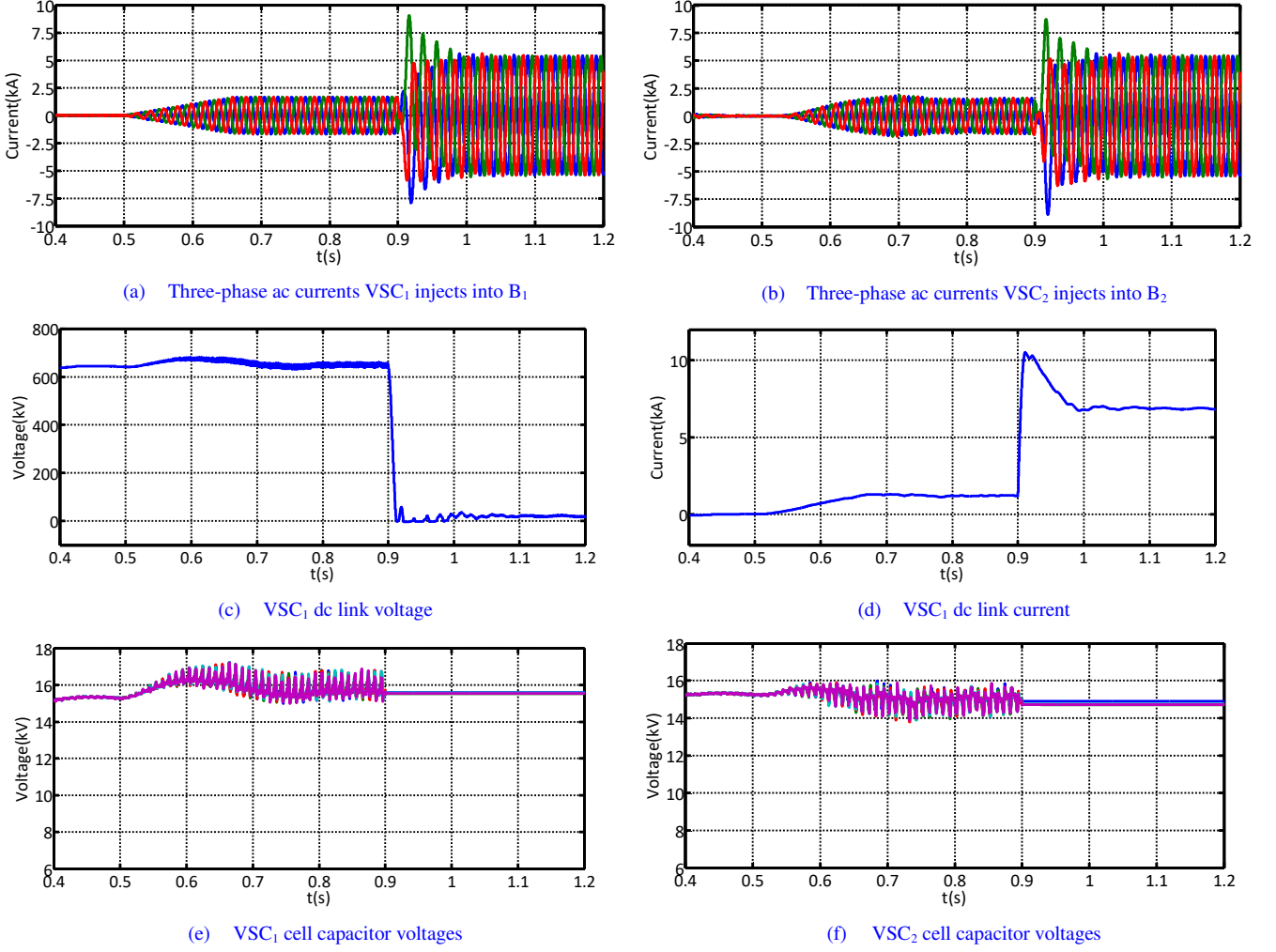


Fig. 10: Simulation waveforms that illustrate the response of the CTB converter based HVDC link to pole-to-pole dc short circuit fault

## V. COMPARISON BETWEEN CONTROLLED TRANSITION BRIDGE AND HALF-BRIDGE MODULAR CONVERTERS

Table I shows high-level comparison between two converters that do not offer dc fault blocking, namely, the CTB and half-bridge modular converters, where,  $I_{dc}$  and  $I_m$  represent dc link current and peak of the output phase current. Observe that although CTB offers small footprint and reduced power circuit and control complexity compared to HB-MMC, its dc fault response is similar to that of the two-level converter. This may limit its applications to the point-to-point HVDC links.

Table II shows the estimate of the on-state losses of the CTB converter and HB-MMC obtained from simulations. The comparison in Table II is carried out when both converters being compared employ 4.5kV IGBTs (T1800GB45A), with 50% device utilization (2.25kV per device). The results in Table II show that the CTB has marginally higher on-state losses than the HB-MMC when it exchanges large active power, and this is due to the influence of the relatively large rebalancing currents associated with the recharge or discharge of the full-bridge cell capacitors from/ and to the dc link. From the sample plot for the voltage across the switching devices of the two-level converter in Fig. 2(c), it is observed that the switching devices of the two-level converter stage of the CTB converter turn on and off at near zero voltage; thus, incur zero switching loss. This means that the entire switching loss in the CTB will come from the three limbs. Taking into account the latter point, the overall semiconductor loss of the CTB converter is expected to be similar to or marginally lower than that of the HB-MMC.

Table I: High level comparison between the CTB converter and half-bridge MMC.

	CTB	HB-MMC
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Number of cell capacitors per phase	$\frac{1}{4}N$	$N$
Number of semiconductor per phase	$N$	$2N$
Number switches in conduction path per phase	$\frac{1}{2}N$ , (with each must be able to handle peak of the output current $I_m$ plus inrush current during clamping of the each limb to positive and negative dc rails)	$N$ (with each device must be able to hand peak current of $\frac{1}{2}I_{dc} + \frac{1}{2}I_m$ )
Efficiency	high	high
Active and reactive power control range	Excellent over full P-Q envelope	Excellent over full P-Q envelope
AC fault ride-through capability	Excellent	Excellent
DC fault survival	worse than half-bridge MMC as the discharge of the dc link capacitors increases the fault level as that in the two-level converter	better

Table II: On-state loss comparison between half-bridge MMC and CTB converter (both converters rated for 640 kV, 300 kV line-to-line ac voltage, and the following switching devices' parameters are:  $V_{T0}=1.82$  V,  $V_{D0}=2.27$  V,  $r_T=1.2$  m $\Omega$  and  $r_D=1.07$  m $\Omega$ )

Converter type	P=800 MW and Q=0	P=800 MW and Q=+300 MVar(capacitive)	P=800 MW and Q=-300 MVar (inductive)	P=0 and Q=+800 MVar (capacitive)
HB-MMC	4.18 MW (0.52%)	4.5 MW (0.56%)	4.50 MW (0.56%)	3.65 MW
CTB	4.25 MW (0.53%)	4.50 MW (0.56%)	5.00 MW (0.625%)	2.10 MW (0.26%)

## VI. CONCLUSION

This paper has utilized multilevel modulation plus 3<sup>rd</sup> harmonic injection to decouple the full-bridge cell capacitor voltage balancing of a controlled transition bridge converter from the modulation index and load power factor. The injected 3<sup>rd</sup> harmonic injection modifies the modulating signal of each phase leg such that each limb of the CTB converter is clamped to the positive and negative dc rail at least once or twice every half fundamental period; thus, allowing the cell capacitor voltages to be balanced, independent of modulation index and load power factor. Open loop simulations have demonstrated the universality of the CTB converter, while its suitability for the HVDC applications was demonstrated using a point-to-point VSC-HVDC link example. The main features of operating the CTB converter in a typical multilevel mode were highlighted.

In summary, the main contributions of this paper are:

- (1). Section 0 of this paper has described the theoretical basis that underpins the operating principle of the CTB converter and identified a number of fundamental issues that hamper its applications in real and reactive power applications beyond that reported in the open literature [23, 28].
- (2). With the aid of 3<sup>rd</sup> harmonic injection, the problem of limited modulation index control range of the CTB converter reported in [23, 28] has been addressed. This is achieved through the manipulation of the discharge period of the cell capacitors (during control transition mode) and charging period of the cell capacitors (during cell capacitor rebalancing mode), see section II.
- (3). Sections II, III and IV presented an approximate method for sizing of the CTB converter cell capacitances, design of the controllers that regulate cell capacitor voltages and limb currents, and presented comprehensive simulations that demonstrate the decoupling of the cell capacitor voltage from the modulation index and power factors, including during normal and abnormal conditions.

## VII. ACKNOWLEDGEMENT

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